PARALLEL INTERFACE ADAPTOR 2200-420 JUNE 10, 1972

Product Specification

Datapoin



DATAPOINT CORPORATION

PRODUCT SPECIFICATION

6/10/72.

PARALLEL INTERFACE ADAPTOR

2200-420

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1.0 GENERAL DESCRIPTION

The DATAPOINT 2200-420 Parallel Interface Adaptor is designed to interface the DATAPOINT 2200 to any peripheral equipment that requires parallel data. The DATAPOINT 2200 interchanges data with all peripherals over the same 8 bit data input/output bus, requiring that devices placed on this bus follow stringent rules as to when and what data is placed on it. The Parallel Interface Adaptor provides for addressing, status and data modes, and data buffering, so that the external device only has to present its outputs and receive its inputs from the Parallel Interface Adaptor. 2.0 SYSTEM REQUIREMENTS

The 2200-420 requires only two cables for operation. One is a standard I/O cable (supplied with 2200-420) between the 2200-420 and the DATAPOINT 2200. Through this cable the 2200-420 receives all operating power and makes the necessary connections to the DATAPOINT 2200 I/O bus. The second cable connects the 2200-420 to the external device to be interfaced. This cable will vary, depending on the characteristics of the external device.

Power for the 2200-420 is derived from the DATAPOINT 2200 for one or two adaptors. Additional adaptors require supplemental power.

3.0 TECHNICAL DESCRIPTION

The 2200-420 has seven major sections:

- 1. DEVICE ADDRESS CONTROL
- 2. DATA INPUT BUFFER/REGISTER
- 3. STATUS INPUT BUFFER/REGISTER
- 4. DATA OUTPUT REGISTER/BUFFER

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- 5. COMMAND REGISTER/BUFFER
- 6. CONTROL STROBE BUFFER
- 7. POWER ON RESET

3.1 Device Address Control

Each 2200-420 connected to the DATAPOINT 2200 I/O bus must have a unique address so that it can determine if the data is meant for it. If the 2200-420 is not currently addressed, all data or status transfer to the DATAPOINT 2200 I/O bus is inhibited. Likewise, the control strobes are inhibited from being sent to the external device. When the 2200-420 is addressed, it will present a "1" on the interface address status output. For the remainder of this technical description, it will be assumed that the 2200-420 is addressed.

The 2200-420 is factory wired for an I/O address of 226_8 . This may be field changed to any other address at any time.

When the 2200-420 is addressed, it will present either the DATA or STATUS of the external device to the DATAPOINT 2200. This is determined by the DATA MODE or STATUS MODE operation of the 2200-420.

The 2200-420 is placed in the STATUS MODE whenever an EX ADDRESS strobe is received from the DATAPOINT 2200. It can also be placed in the STATUS MODE without re-addressing by receiving an EX STATUS strobe. When in the STATUS MODE the 2200-420 will present to the DATAPOINT 2200 the information contained in the STATUS INPUT REGISTER.

The 2200-420 can be placed in the DATA MODE by an EX DATA strobe from the DATAPOINT 2200. When in the DATA MODE, the 2200-420 will present to the DATAPOINT 2200 the information contained in the DATA INPUT REGISTER.

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If the 2200-420 is not addressed, it will not respond to any commands from the DATAPOINT 2200 nor will it return any data or status to the DATAPOINT 2200.

3.2 Data Input Buffer/Register

The eight data inputs to the 2200-420 from the external device are received by high-impedance differential comparators. The input impedance is about 15K ohms and the inputs are overvoltage protected and integrated for noise rejection. The decision level is +2.4 volts ±0.3 volts. The DATA INPUT REGISTER can be latching or non-latching. If the latching mode is chosen, the DATA INPUT REGISTER will hold the data present at the data input terminals when input status bit S7 is strobed.

3.3 Status Input Buffer/Register

The STATUS INPUT BUFFER/REGISTER is an 8-bit register intended to hold status information from the external device (xmit ready, receive ready, etc.). The STATUS INPUT REGISTER can be made latching or non-latching. If the latching mode is chosen, status bits 0 - 6 will be reset upon the execution of any INPUT instruction by the DATAPOINT 2200 while the 2200-420 is in the STATUS MODE (see STATUS/DATA -Section 3.1). Status bit 7 can be reset at the same time as bits 0 - 6 or optionally by the execution of an INPUT instruction while in the DATA MODE. The inputs of the STATUS INPUT BUFFER have the same electrical characteristics as the DATA INPUT BUFFERS (Section 3.2). 3.4 Data Output Register/Buffer

The DATA OUTPUT REGISTER/BUFFER is an 8-bit register to hold data from the DATAPOINT 2200 to the external device. This register is set to the contents of the I/O bus at the execution of an EX

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WRITE instruction by the DATAPOINT 2200. The contents of the DATA OUTPUT REGISTER/BUFFER will not change until the execution of the next EX WRITE instruction by the DATAPOINT 2200.

The DATA OUTPUT BUFFER is an open collector TTL gate, making the outputs TTL compatible. At the ground state it will sink approximately 35 ma and in the high state it will source about 1 ma. A low output is between 0 and +.4 volts; a high output is +5 or +12, depending on the option selected.

3.5 Command Register/Buffer

The COMMAND REGISTER is an 8-bit register typically used to send a command word to the external device. This register is set to the contents of the DATAPOINT 2200 I/O bus when an EX COMI instruction is executed by the DATAPOINT 2200. The COMMAND REGISTER will not change until another EX COMI is executed.

The electrical characteristics of the COMMAND BUFFER are the same as the DATA OUTPUT BUFFER (Section 3.4).

3.6 Control Strobe Buffer

The following control strobes are gated to occur only while the 2200-420 is addressed. They are buffered to provide the same electrical characteristics as the DATA OUTPUT BUFFER (Section 3.4).

SENSE STATUS - also puts PARALLEL INTERFACE in STATUS MODE SENSE DATA - also puts PARALLEL INTERFACE in DATA MODE WRITE - also loads DATA OUTPUT REGISTER COM1 - also loads COMMAND REGISTER COM2 COM3 COM4

3.7 Power On Reset

When system power is applied (by turning on the DATAPOINT 2200) the DATA OUTPUT REGISTER and COMMAND REGISTER are set to "0" and a one millisecond pulse occurs on the system reset strobe.

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This pulse may be used to initiate the external device at power on.

4.0 PHYSICAL DESCRIPTION

See Figure 1 for outline drawing.

5.0 ENVIRONMENTAL REQUIREMENTS

0° to 50°C (32° to 122°F)

10 to 95% relative humidity

6.0 INTERFACE REQUIREMENTS

See Figure 2 for pin connections and signal names.

7.0 OPTIONS

The following options are fully strappable and changes in configuration may be made by a technician in the field as desired. Factory preparation straps those options noted as standard. prior to shipment.

7.1 Data Inputs (from external device)

- a) latching (on S₇) (E23-E24 jumpered)
- b) non-latching (pass-thru mode) (standard) (E23,E24 open)
- c) ground true (standard) (E1-E2[E3 open])
- d) high true (E3-E2 [El open])

7.2 Status Input (from external device)

a) latching (standard) (E7-E8/E9-E10/E11-E12/E13-E14/E15-E16/

E17-E18/E19-E20 pairs jumpered)

- b) reset S₇ in data mode (standard) (E56-E57 [E55 open])
- c) reset S₇ in status mode (E56-E55 [E57 open])
- d) non-latching (jumpers in "a" above open)
- e) ground true (standard) (E4-E5 [E6 open])
- f) high true (E5-E6 [E4 open])

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- a) high = +5 volts (standard) (E35-E34 [E36 open])
- b) high = +12 volts (E35-E36 [E34 open])

7.4 Data Outputs

- a) ground true (standard) (E41-E40 [E42 open])
- b) high true (E42-E41 [E40 open])
- 7.5 Command Outputs
 - a) ground true (standard) (E37-E38 [E39 open])
 - b) high true (E38-#39 [E37 open])

7.6 Control Strobes

- a) ground true (standard) (E25-E26 [E27 open])
- b) high true (E26-E27 [E25 open])

7.7 System Reset Strobe

- a) high for reset (E29-E30 [E28 open])
- b) low for reset (standard) (E28-E29 [E30 open])

7.8 Interface Address Status

- a) high for addressed (E33-E32 [E31 open])
- b) low for addressed (standard) (E31-E32 [E33 open])
- 7.9 Address
 - a) any address optional (see below)
 - b) standard address is 226



TOP VIEW



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FIGURE 1 2200-420 HOUSING

FIGURE 2

DATAPOINT 2200-420 EXTERNAL DEVICE PIN ASSIGNMENT-J3

PIN NO.	FUNCTION	DESCRIPTION
$\frac{1}{2}$	D0	
3	D2	
4	D3 D4	Data from external devices
6	D5	
7	D6	
8		
10		
11	SI	
12	S2	
13 14	S3 S4	Status from external device
15	S5	
16	S 6	
17	S7 -	(May be used to strobe data later)
18		
20	Sense Status Strobe	Signifies that status word is on A
20		bus input
21	Sense Data Strobe	Signifies that data word is on A bus
22	Write Strobe	Signifies that A bus output is in
23	Command 1 Strobe	Signifies that A bus output is in
2.4	Command 2 Strobe	Command Buller
25	Command 3 Strobe	Other available external strobes
27 28	System Reset Strobe	Power-on-reset
29	Interface Address Status	Signifies that interface is addressed
30	NC	
31 32	Ground Ground	Signal and power referenced
33	NC	
34	DOO	
35	DOL	
30 27		Data to external devices
38		Data to externar devices
39	D05	
40	DO6	
41	DO7	
42	NC	

FIGURE 2

DATAPOINT 2200-420 EXTERNAL DEVICE PIN ASSIGNMENT-J3 (Continued)

PIN NO.	FUNCTION	DESCRIPTION
43 44 45 46 47 48 49 50	C0 C1 C2 C3 C4 C5 C6 C7	Command word to external device







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8.0 PARTS LIST

The following separate parts are part of the 2200-420 and are included in each shipment:

Quantity	Description
1	2200-420 Parallel Interface Adaptor
1	2200-160 Universal I/O Cable
1	2200-436 Connector Kit
1	Reference Manual
1	Test Tape Cassette
1	Test Connector